Low Power *XOR* Gate Decomposition

Prof. Igor Murashko, e-mail: iamurashko@tut.by
Department of Information Technologies
Pavel Sukhoi State Technical University of Gomel, Gomel, Belarus

Currently, the power consumption is one of the most important concerns of *VLSI* design [1]. Three factors mainly contribute to this trend. Firstly, without low-power design techniques, future mobile devices will have limited battery life or heavy battery pack. Secondly, power dissipation in high-speed devices leads to increase the packaging and cooling costs. Thirdly, all modern *VLSI* has built-in self testing hardware. This hardware practically don't use in normal mode operation. But during testing they use very intense. In [2] was shown that power dissipation during testing was increasing in 2-3 times. Therefore, low-power techniques are very actual problem.

Modulo two adders are widely used in a variety of digital circuits such as specialized calculators, communication circuits, error correcting circuits, pseudorandom numbers generators, signature analyzers, etc. In this work a problem low-power decomposition of *XOR* based circuits are considered.

The dominant source of power dissipation in *CMOS* circuits is dynamic power dissipation. They consist of two components: charging and discharging of the node capacitances (also referred to as the capacitive power dissipation) and short-circuit current between the supply rails during output transitions. The dynamic power dissipation is given by [3]:

$$P = {}^1\!/_2 V_{dd}^2 f_{CLK} \sum_{i=1}^{n} C_L^i \cdot WSA_i \ ,$$

where V_{dd} – is the supply voltage, f_{CLK} – is the clock frequency, C_L^i – is the load capacitance at the output of gate, WSA_i – is the expected number of transitions per clock cycle (referred to as weighted switching activity, or *WSA*), n – number of nodes.

In this work next the following notation are used [3]: load capacitance of every nodes is equal; supply voltage and clock frequency is constant; gate delays are assumed to zero. Thus for power estimation it is necessary to calculate weighted switching activity for every node. Technique for calculated *WSA* was proposed in [4]. The main idea of this technique consists of different time for switching for every node. So every input switching translates onto output (fig.1).

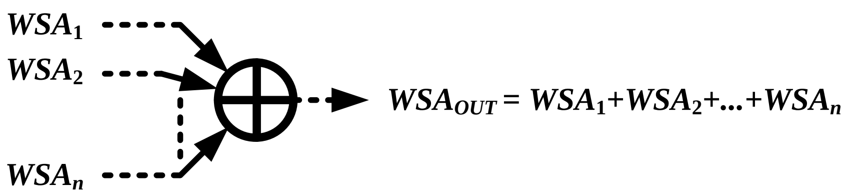


Fig.1. *WSA* Estimation of multiple-input modulo two adders

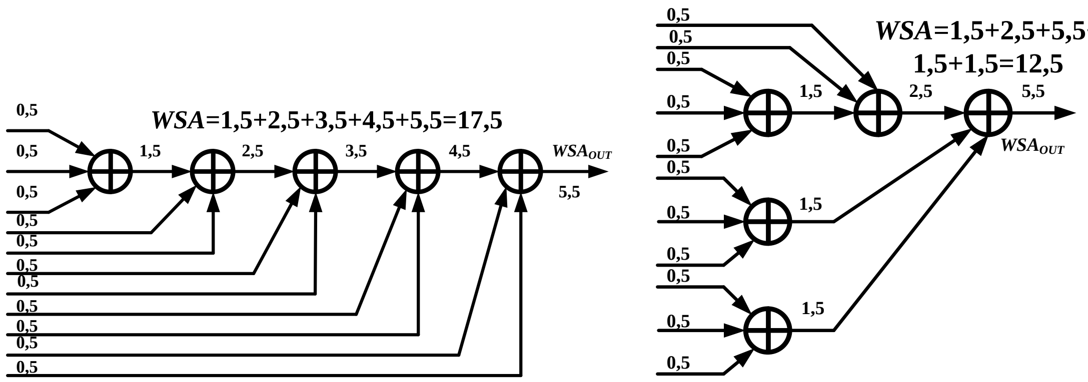
Technology decomposition is the step before technology mapping which decompose multiple-input logical elements into a network with only two-input gates (three, four, and all). In [4] was described a problem of decomposition a multi-input *XOR* gate into a tree of two-input *XOR* gates. But technology library contain different primitives such as two, tree, four, eight input gates (as example, library A*MI350HXGC* contain only two and tree input *XOR* gates [5]). In this work we consider decomposition multiple-input logical elements into a network with any input gates.

Let n is number of inputs multiple-input modulo two adders, d number of inputs gate. Number of gates (k), which is needed for making n-input logical element on d-input gates, is calculated as:

$$k = \left\lceil \frac{n-1}{d-1} \right\rceil,$$

where $\lceil x \rceil$ – is nearest integer, greatest or equal *x*.

As has shown in [3], exist many different variants of decomposition multi-input logical elements. This variant has equal number of gates but different switching activity. Figure 2 shown examples decomposition 11-input modulo two adders into a network with tree-input *XOR* gates. Both circuits have equal number of gates. But second circuit has switching activity in 1.4 time's less than first circuit.



a) *b)*

Fig.2. Decomposition of 11-input element:
a – with maximal *WSA*, *b* – with minimal *WSA*

For the synthesis of multi-input *XOR*-based circuits with minimal switching activity can be used the following recursive algorithm (assume that switching activity for any input is equal 0.5, number of inputs gate *d*=3). First calculate output switching activity $WSA_{out} = 0{,}5 \cdot n$ and temporary variable $WSA_d = 3 \cdot 0{,}5 = 1{,}5$. Then imagine WSA_{out} as the sum of the 3 numbers $WSA_{out} = WSA_1 + WSA_2 + WSA_3$ so that for 2 of 3 variable WSA_i ($i = \overline{1,3}$) the result of dividing WSA_i by WSA_d was integer. Moreover it is necessary following conditions $|WSA_i - WSA_j| = 0$, $|WSA_i - WSA_j| = 0{,}5$ or $|WSA_i - WSA_j| = 1{,}0$, where $i = \overline{1,3}$, $j = \overline{1,3}$, $i \neq j$. This step repeat for all nodes until $WSA_i \neq 0{,}5$.

The result of algorithm for *n*=11, *d*=3 was shown on fig.2, b. This algorithm easy can be modified for any gates.

This work is dealing to a problem of decomposition multiple input *XOR*-based circuits. Different variants of decomposition have different switching activity they characterizing power dissipation. An algorithm for synthesis of multi-input *XOR*-based circuits with minimal switching activity was proposed. This algorithm can be used in computer-aided environment.

References:

1. Roy K. and Prasad S.C. Low power CMOS VLSI circuit design. – New York: John Wiley and Sons, Inc., 2000. – 376 p.

2. Zorian Y. A Distributed BIST Control Scheme for Complex VLSI Devices.Proc. 11th IEEE VLSI Test Symposium, May1993. – P. 4-9.

3. Murashko I. and Yarmolik V. Built-In Self-Testing: A power reduction methods. – Saarbrucken: LAP LAMBERT Academic Publishing, 2012. – 339 p. [in Russian]

4. Murashko I. Power consumption analysis of XOR based circuits. – Informatics. – 2006, №1 (9). – P.97-103. [In Russian]

5. 0,35 Micron CMOS Gate Array Data Book AMI350HXGC 3,3 Volt (Revision 1.0). – AMI Semiconductors, Inc. – 2002.